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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Edward A. Burton et al.

Title: APPARATUS AND METHOD TO CONTROL SELF-TIMED AND SYNCHRONOUS SYSTEMS

Docket No.: 884.C02US1
Filed: December 31, 2003
Examiner: Anh-Quan Tra

Serial No.: 10/750,320
Due Date: April 1, 2006 (Saturday)
Group Art Unit: 2816

MS Appeal Brief - Patents
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APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Edward A. Burton et al. Examiner: Anh-Quan Tra

Serial No.: 10/750,320 Group Art Unit: 2816

Filed: December 31, 2003 Docket: 884.C02US1

For: APPARATUS AND METHOD TO CONTROL SELF-TIMED AND SYNCHRONOUS SYSTEMS

Assignee: Intel Corporation

APPEAL BRIEF UNDER 37 CFR § 41.37

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on January 23, 2006, from the Final Rejection of claims 1-20 and 26-30 of the above-identified application, as set forth in the Final Office Action mailed on September 22, 2005.

The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of 500.00 which represents the requisite fee set forth in 37 C.F.R. § 41.2(b)(2). The Appellant respectfully requests consideration and reversal of the Examiner's rejections of the pending claims.

1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, INTEL CORPORATION.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

The present application was filed on December 31, 2003 with claims 1-30. A non-final Office Action was mailed on June 14, 2005. A Final Office Action (hereinafter the "Final Office Action") was mailed on September 22, 2005. A Notice of Panel Decision from Pre-Appeal Brief Review was mailed on March 1, 2006. Claims 1-20 and 26-30 stand twice rejected, remain pending, and are the subject of the present Appeal.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Final Office Action dated September 22, 2005.

5. SUMMARY OF CLAIMED SUBJECT MATTER

Some aspects of the present inventive subject matter include, but are not limited to, apparatus, systems, and methods. One or more embodiments may include, as illustrated for example but not limited to Fig. 1A, an apparatus comprising a substrate 102, a target timing circuit 104 formed on the substrate, the target timing circuit having a frequency related to a target frequency (page 4, lines 27-28), a leakage timing circuit 106 formed on the substrate, the leakage timing circuit having a frequency related to a leakage current (page 4, lines 29-30), and a control unit 108 to maintain a substantially constant ratio between the frequency related to the target frequency and the frequency related to the leakage current (page 3, lines 21-23, page 4, lines 22-24).

One or more embodiments may include, as illustrated for example but not limited to Fig. 2, a system 200 comprising a substrate 102, a target timing circuit 104 formed on the substrate, the target timing circuit having a frequency related to a target frequency (page 4, lines 27-28), a leakage timing circuit 106 formed on the substrate, the leakage timing circuit having a frequency related to a leakage current (page 4, lines 29-30), a control unit 108 coupled to a flash memory 204 and to maintain a substantially constant ratio between the frequency related to the target frequency and the frequency related to the leakage current (page 3, lines 21-23, page 4, lines 22-24), and a self-timed circuit 124 formed on the substrate, and the self-timed circuit to operate at a frequency proportional to the target frequency (page 6, lines 30-31).

One or more embodiments may include, as illustrated for example but not limited to Fig. 1D, an apparatus comprising a substrate 102, a self-timed circuit 124 formed on the substrate, the self-timed circuit to operate at a target circuit frequency (page 6, lines 21-31), a target timing circuit 104 formed on the substrate, the target timing circuit to generate a signal having a frequency related to the target circuit frequency(page 4, lines 27-28), a leakage timing circuit 106 formed on the substrate, the leakage timing circuit having a leakage current and the leakage timing circuit to generate a signal having a frequency related to the leakage current (page 3, lines 21-23, page 4, lines 22-24), and a

control unit 108 to receive the signal having the frequency related to the target circuit frequency and the signal having the frequency related to the leakage current and to generate a control signal for application to the substrate, the control signal to maintain a substantially constant ratio between the frequency related to the target circuit frequency and the frequency related to the leakage current (page 3, lines 11-23, page 4, line 22-24, page 6, line 30 through page 7, line 3).

One or more embodiments may include, as illustrated for example but not limited to Fig. 1A and Fig. 4A, an apparatus 400 comprising a substrate 102, a synchronous circuit 414 formed on the substrate, the synchronous circuit to operate at a target circuit frequency, a target timing circuit 104 formed on the substrate, the target timing circuit including voltage control, the target timing circuit to generate a signal having a frequency related to the target circuit frequency, a leakage timing circuit 106 formed on the substrate, the leakage timing circuit including voltage control, the leakage timing circuit having a leakage current and the leakage timing circuit to generate a signal having a frequency related to the leakage current, a control unit 108 to receive the signal having a frequency related to the target circuit frequency, the signal having a frequency related to the leakage current, and to generate a control signal for application to the substrate, the control signal to maintain a substantially constant ratio between the frequency related to the target circuit frequency and the frequency related to the leakage current, a power source 410 to provide a potential to the synchronous, the target timing circuit, and the leakage timing circuit, and a potential control unit 412 to receive the signal having the frequency related to the target circuit frequency and the signal having the frequency related to the leakage current and to generate a potential control signal to provide to the power source to adjust the potential. Page 10, line 7 through page 11, line 13.

One or more embodiments may include, as illustrated for example but not limited to Fig. 3, a method (300) comprising generating a first signal related to a target circuit frequency (302), generating a second signal related to a leakage current (304), and adjusting a control signal applied to a substrate to maintain a substantially constant frequency ratio between the first signal and the second signal (306). Page 9, line 23-29.

This summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and its legal equivalents for a complete statement of the invention.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-2, 6-18, 26-27, and 29 were rejected under 35 U.S.C. § 102(b) as being anticipated by Mizuno et al. (U.S. 6,166,577).

Claims 3-5 and 19-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Mizuno et al. (U.S. 6,166,577) in view of Klemmer (U.S. 6,337,601).

Claims 28 and 30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Mizuno et al. (U.S. 6,166,577).

7. ARGUMENT

A) The Applicable Law under 35 U.S.C. §102(b)

Anticipation under 35 U.S.C. § 102 requires the disclosure in a single prior art reference of each element of the claim under consideration. *See Verdegaal Bros. V. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). It is not enough, however, that the prior art reference discloses all the claimed elements in isolation. Rather, "[a]nticipation requires the presence in a single prior reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added). "The *identical invention* must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP § 2131 (emphasis added).

B) Discussion of the rejection of claims 1-2, 6-18, 26-27, and 29 under 35 U.S.C. § 102(b) as being anticipated by Mizuno et al. (U.S. Patent No. 6,166,577).

Claims 1-2, 6-18, 26-27, and 29 were rejected under 35 U.S.C. § 102(b) as being anticipated by Mizuno et al. (U.S. 6,166,577). Appellant believes there is a clear deficiency in the *prima facie* case in support of the rejection, namely, that the Final Office Action has not shown that Mizuno et al. discloses the identical invention as claimed. Appellant respectfully traverses the rejection of claims 1-2, 6-18, 26-27, and 29.

Appellant's previous response (mailed August 12, 2005, hereinafter the "Previous Response") to a non-final Office Action mailed on June 14, 2005 in this matter on pages 8-9 states,

> Claims 1 and 12 recite, "a leakage timing circuit formed on the substrate, the leakage timing circuit having a frequency related to a leakage current." Claim 16 recites, "a leakage timing circuit formed on the substrate, the leakage timing circuit having a leakage current and the

leakage timing circuit to generate a signal having a frequency related to the leakage current." Claim 26 recites, "generating a second signal related to a leakage current."

In contrast, Mizuno et al. discloses at column 8, lines 4-11 that, "The semiconductor integrated circuit device includes a main circuit LOG1 and a substrate-bias dependent oscillation circuit OSC1 which varies the oscillation frequency in response to the substrate bias. A substrate bias control circuit CNT1 uses the output S1 of the oscillation circuit OSC1 and the oscillation output CLK1 of an operation-mode dependent oscillation circuit VCLK1 to produce substrate voltages BP1 and BN1 for the main circuit LOG1." Thus, Mizuno et al. discloses a substrate-bias dependent oscillation circuit and an operation mode dependent oscillation circuit. However, Mizuno et al. fails to describe a leakage timing circuit having a frequency related to a leakage current as recited in claims 1, 12, and 16, and further, fails to describe generating a second signal related to a leakage current as recited in claim 26. Therefore, Mizuno et al. fails to describe all of the elements recited in claims 1, 12, 16, and 26.

The Office Action on page 2 states, ". . . (the leakage current of the transistor is determined by voltage that is biased to it substrate or well. Therefore, the frequency of OSC circuit is also dependent on the leakage current of the transistor." Applicant respectfully disagrees. The Office Action has pointed to no portion of Mizuno et al. that supports these statements. In addition, Applicant realized that inherent characteristics may be used in forming a rejection based on anticipation, however, to serve as an anticipation when a reference is silent about the asserted inherent characteristic, the gap in the reference may be filled with recourse to extrinsic evidence. But, such evidence must make clear that "the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. v. Monsanto Co.,* 20 USPQ2d 1746, 1749 (Fed. Cir. 1991). Applicant respectfully submits that the Office Action fails to produced any evidence to show that the elements of a leakage timing circuit having a frequency related to a leakage current (as recited in claims 1, 12, and 16) and generating a second signal related to a leakage current (as recited in claim 26) are necessarily present in Mizuno et al. Thus, the Office Action fails to show in a single reference, either explicitly or inherently, all of the elements recited in claims 1, 12, 16, and 26.

In response to these arguments, the Final Office Action on page 6 relies on Mazakaki et al. (USP 6489833) and Teraoka et al. (USP 6333571) to support the statement, "The above examples demonstrate that it is inherent that substrate bias voltage

determines the leakage current of transistor." While Appellant does not necessarily agree with the statement, even if true, the statement still fails to show how any of these references teach, for example, "a leakage timing circuit formed on the substrate, the leakage timing circuit having a frequency related to a leakage current," as recited in claims 1 and 12.

Further, the Final Office Action fails to show how any of these references teach for example, "a leakage timing circuit formed on the substrate, the leakage timing circuit having a leakage current and the leakage timing circuit to generate a signal having a frequency related to the leakage current," as recited in claim 16, and fails to show how any of these references teaches "generating a second signal related to a leakage current," as recited in claim 26.

Because Mizuno et al. fails to show in a single prior reference a disclosure of each and every element of the claimed invention, arranged as in at least claims 1, 12, 16, and 26, the Final Office Action fails to state a *prima facie* case of anticipation with respect to claims 1, 12, 16, and 26.

Claims 2 and 6-11 depend from claim 1, claims 13-15 depend from claim 12, claims 17-18 depend from claim 16, and claims 27 and 29 depend from claim 26. Therefore, dependent claims 2, 6-11, 13-14, 17-18, 27, and 29 include all of the elements recited in the claim from which they depend. For reasons analogous to those stated above and elements in the claims, Appellant respectfully submits that the Final Office Action fails to state a *prima facie* case of anticipation with respect to claims 2, 6-11, 13-15, 17-18, 27, and 29.

For at least the reasons stated above, the Final Office Action fails to state a *prima facie* case of anticipation with respect to claims 1-2, 6-18, 26-27, and 29. Therefore, Appellant respectfully requests withdrawal of the rejection and reconsideration and allowance of claims 1-2, 6-18, 26-27, and 29.

C) The Applicable Law under 35 U.S.C. §103

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). As part of establishing a *prima facie* case of obviousness, the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *Id.*

The court in *Fine* stated that:

> Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 878 (CCPA 1981)). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys.*, 732 F.2d at 1577, 221 USPQ at 933. And "teachings of references can be combined *only* if there is some suggestion or incentive to do so."

Id. (emphasis in original).

The M.P.E.P. adopts this line of reasoning, stating that

> "To establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991))". *M.P.E.P.* § 2142.

The test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985). The Examiner must, as one of the inquiries

pertinent to any obviousness inquiry under 35 U.S.C. § 103, recognize and consider not only the similarities but also the critical differences between the claimed invention and the prior art. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990), *reh'g denied*, 1990 U.S. App. LEXIS 19971 (Fed. Cir. 1990). Further, the Office Action must provide specific, objective evidence of record for a finding of a suggestion or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *In re Sang Su Lee*, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002). Further yet, the fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP § 2143.01. Finally, the Examiner must avoid hindsight. *In re Bond* at 834.

D) Discussion of the rejection claims 3-5 and 19-20 under 35 U.S.C. § 103(a) as being unpatentable over Mizuno et al. (U.S. 6,166,577) in view of Klemmer (U.S. 6,337,601).

Claims 3-5 and 19-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Mizuno et al. (U.S. 6,166,577) in view of Klemmer (U.S. 6,337,601). Appellant respectfully traverses the rejection of claims 3-5 and 19-20.

The proposed combination of Mizuno et al. with Klemmer fails to describe or suggest all of the elements of claims 3-5 and 19-20.

Claims 3-5 depend from claim 1, and claims 19-20 depend from claim 16. Therefore, dependent claims 3-5 and 19-20 include all of the elements of the claim from which they depend. Appellant believes they have established that Mizuno et al. fails to describe or suggest all of the elements of claims 1 and 16, and so also fails to describe or suggest all of the elements of dependent claims 3-5 and 19-20. Klemmer also fails to supply these elements missing from Mizuno et al. as recited in claims 1 and 16.

Therefore, the proposed combination of Mizuno et al. and Klemmer fails to describe or suggest all of the elements of claims 3-5 and 19-20.

Further, dependent claims 3-5 and 19-20 recite additional elements that are not described or suggested by the proposed combination of Mizuno et al. and Klemmer. For example, claim 5 recites, "wherein the frequency related to the leakage current is substantially proportional to the leakage current." The Final Office Action on page 5 states, "Mizuno et al.'s figure 12 shows that the frequency related to the leakage current is substantially proportional to the leakage current." Appellant respectfully disagrees. FIG. 12 of Mizuno et al. merely depicts various blocks connected together, and fails to show any description or suggestion of the frequencies that may or may not be associated with these blocks. Further, as argued above, Mizuno et al. fails to describe or suggest a relationship between a leakage current and a frequency related to the leakage current. Therefore, FIG. 12 of Mizuno et al. also fails to describe or suggest "wherein the frequency related to the leakage current is substantially proportional to the leakage current," as recited in claim 5.

In response to that argument, the Final Office Action on page 6 states, "Such characteristic is inherent in Mizuno et al.'s circuit because the threshold of the transistor is related to the leakage current of the transistor, and the speed of the transistor is related to the threshold of the transistor." (Emphasis added).

Appellant disagrees. And while Appellant does not admit that this statement is true, the statement still fails to show how the proposed combination of references teaches or suggests a frequency related to the leakage current. Appellant also submits that the "speed of a transistor" fails to teach or suggest a frequency related to the leakage current substantially proportional to the leakage current, as recited in claim 5. Thus, Appellant maintains that the Final Office Action fails to provide any evidence to show that frequency is related to the leakage current, or that such a characteristic is inherent in Mizuno et al. because of the statement that the threshold of the transistor is related to the leakage current of the transistor, and the speed of the transistor is related to the threshold of the transistor.

Thus, the proposed combination of Mizuno et al. with Klemmer fails to supply these elements missing from Mizuno et al. Therefore, the proposed combination of Mizuno et al. and Klemmer fails to describe or suggest all of the elements recited in claim 5.

The Final Office Action fails to provide a proper basis for forming the proposed combination of Mizuno et al. with Klemmer.

The Final Office Action fails to provide specific, objective evidence of record for a finding of a description, suggestion, or motivation to combine Mizuno et al. with Klemmer. The Final Office Action on page 4 states, "However, Klemmer's figure 3 shows a timing circuit having counter 82 coupled to the ring oscillator 80 for the purpose of increasing output frequency. Therefore, it would have been obvious to one having ordinary skill in the art to add a counter coupled between the oscillator OSC10 and CNT10 for the purpose of increasing the output frequency of the oscillator OSC10." Appellant respectfully disagrees.

In Mizuno et al., the stated purpose of supplying the substrate bias voltages BP1 and BN1 to the oscillator OSC1 is disclosed at column 8, lines 29-38 where it states:

> The substrate bias voltages BP1 and BN1 are also supplied to the substrate-bias dependent oscillation circuit OSC1. The substrate-bias dependent oscillation circuit OSC1 and the substrate bias control circuit CNT1 which receives the output S1 of the oscillation circuit OSC1 as a feedback signal form a stable negative feedback system so that the output S1 of the oscillation circuit OSC1 has its frequency locked to the frequency of oscillation output CLK1 of the operation-mode dependent oscillation circuit VCLK1.

Thus, Mizuno et al. is concerned with locking the frequency of the OSC1 oscillator to the frequency of the output CLK1. FIG. 12 of Mizuno et al. uses the same single CLK10 output to adjust the output frequencies of individual oscillators OSC10-OSC30. (*See* Mizuno et al. at column 14, lines 47-60). However, there is no description or suggestion in Mizuno et al. of connecting a counter between OSC10 and CNT10 for

the purpose of "increasing the output frequency of the oscillator OSC10" as suggested in the Final Office Action. Increasing the output frequency of the OSC10 oscillation circuit would actually destroy the stated purpose in Mizuno et al. of "locking the frequency of the OSC1 oscillator to the frequency of the output CLK1." Therefore, the statements in the Final Office Action are unsupported by the cited documents, and merely represent reconstruction of the Appellant's claimed invention using impermissible hindsight. Thus, the Final Office Action fails to provide specific, objective evidence of record for a finding of a description, suggestion, or motivation to combine Mizuno et al. with Klemmer.

In response to these arguments, the Final Office Action on page 6 states, "One skilled in the art would have been motivated to add a frequency divider (counter) to Mizuno et al.'s circuit in order to increase the OSC's frequency N time the CLK1's frequency." Appellant disagrees. Further, the statement is not supported by the cited references, and still further, as noted above, the statement destroys the stated purpose in Mizuno et al. of locking the frequency of the OSC1 oscillator to the frequency of output CLK1. Thus, one or ordinary skill in the art would not be motivated to add a frequency divider to the Mizuno et al. circuit in order to increase the OSC's frequency N time the CLK1's frequency, as suggested in the Final Office Action.

By failing to provide a specific, objective evidence of record for a finding of a description, suggestion, or motivation to combine Mizuno et al. with Klemmer, the Final Office Action fails to state a *prima facie* case of obviousness with respect to claims 3-5 and 19-20.

For at least the reasons stated above, the Final Office Action fails to state a *prima facie* case of obviousness with respect to claims 3-5 and 19-20. Therefore, Appellant respectfully requests withdrawal of the rejection and reconsideration and allowance of claims 3-5 and 19-20.

E) Discussion of the rejection claims 28 and 30 under 35 U.S.C. § 103(a) as being unpatentable over Mizuno et al. (U.S. 6,166,577).

Claims 28 and 30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Mizuno et al. (U.S. 6,166,577). Appellant respectfully traverses the rejection of claims 28 and 30.

The cited reference of Mizuno et al. fails to describe or suggest all of the elements of claims 28 and 30.

Claims 28 and 30 depend from claim 26. Therefore, dependent claims 28 and 30 include all of the elements recited in claim 26. Appellant believes they have established that Mizuno et al. fails to describe or suggest all of the elements of claim 26, and so also fails to describe or suggest all of the elements of dependent claims 28 and 30.

In addition, claims 28 and 30 each recite, "further comprising for a communications circuit formed on the substrate, activating a transceiver in the communications circuit." The Final Office Action admits on page 5 that Mizuno et al. fails to show a communication circuit formed on a substrate. Further, the Final Office Action on page 5 states, "Therefore, it would have been obvious to one having ordinary skill in the art to use Mizuno et al's figure 12 in a communication circuit for the purpose of reducing power consumption."

Appellant respectfully disagrees. Since the Final Office Action fails to cite any additional references that describe or suggest a communication circuit formed on the substrate, activating a transceiver in the communication circuit, as recited in claims 28 and 30, Appellant assumes the Final Office Action is taking official notice of these missing elements. Appellant has traversed the taking of official notice and requested that the Examiner provide a reference that describes the elements as recited in claims 28 and 30. However, such a reference has not been provided. Nor has an affidavit, as required by MPEP § 2144.03, been provided. Because no reference or affidavit as noted above has been provided, Appellant requests withdrawal of the rejection and reconsideration and allowance of claims 28 and 30.

Further, and in response to these arguments, the Final Office Action on page 7 refers to USP 6067612 figure 2, and USP 6044937 figure 1. However, the Final Office Action fails to point out where these references teach or suggest the elements as recited in claims 28 and 30. Further, the Final Office Action fails to provide any teaching of a motivation or suggestion to combine these references with the references used in making the rejection of claims 28 and 30. Still further, the Final Office Action, like the previous Office Action, fails to show how "it would have been obvious to one having ordinary skill in the art to use Mizuno et al. in communication circuit for the purpose of saving power consumption," as recited on page 7 of the Final Office Action.

For at least the reasons stated above, the Final Office Action fails to state a *prima facie* case of obviousness with respect to claims 28 and 30. Therefore, Appellant respectfully requests withdrawal of the rejection and reconsideration and allowance of claims 28 and 30.

8. SUMMARY

For at least the reasons argued above, claims 1-2, 6-18, 26-27, and 29 were not properly rejected under 35 U.S.C. § 102(b) as being unpatentable over Mizuno et al., claims 3-5 and 19-20 were not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Mizuno et al. in view of Klemmer, and claims 28 and 30 were not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Mizuno et al.

It is respectfully submitted that the documents cited do not render claims 1-20 and 26-30 anticipated or obvious, and that the claims are patentable over the cited documents. Reversal of the rejections and allowance of the pending claims is respectfully requested.

Respectfully submitted,

EDWARD A. BURTON et al.

By their Representatives,

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Date APRIL 3/2006 By Robert Madden

Robert Madden
Reg. No. 57,521

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ROBERT MADDEN Robert Madden

Name Signature

CLAIMS APPENDIX

1. (Rejected) An apparatus comprising:

a substrate;

a target timing circuit formed on the substrate, the target timing circuit having a frequency related to a target frequency;

a leakage timing circuit formed on the substrate, the leakage timing circuit having a frequency related to a leakage current; and

a control unit to maintain a substantially constant ratio between the frequency related to the target frequency and the frequency related to the leakage current.

2. (Rejected) The apparatus of claim 1, wherein the substrate comprises a semiconductor.

3. (Rejected) The apparatus of claim 2, wherein the target timing circuit comprises a ring oscillator coupled to a counter.

4. (Rejected) The apparatus of claim 3, wherein the leakage timing circuit comprises a ring oscillator.

5. (Rejected) The apparatus of claim 4, wherein the frequency related to the leakage current is substantially proportional to the leakage current.

6. (Rejected) The apparatus of claim 1, further comprising a self-timed circuit formed on the substrate, the self-timed circuit to operate at a frequency proportional to the target frequency.

7. (Rejected) The apparatus of claim 6, the control unit to provide a control signal to the substrate.

8. (Rejected) The apparatus of claim 6, wherein the substrate includes a plurality of coupled wells containing transistors of a matching type from the self-timed circuit, the target timing circuit, and the leakage timing circuit.

9. (Rejected) The apparatus of claim 8, wherein the transistors are all of the matching type.

10. (Rejected) The apparatus of claim 9, further comprising a well control unit to provide a bias to the plurality of coupled wells.

11. (Rejected) The apparatus of claim 10, wherein the well comprises a p-type well.

12. (Rejected) A system comprising:

a substrate;

a target timing circuit formed on the substrate, the target timing circuit having a frequency related to a target frequency;

a leakage timing circuit formed on the substrate, the leakage timing circuit having a frequency related to a leakage current;

a control unit coupled to a flash memory and to maintain a substantially constant ratio between the frequency related to the target frequency and the frequency related to the leakage current; and

a self-timed circuit formed on the substrate, and the self-timed circuit to operate at a frequency proportional to the target frequency.

13. (Rejected) The system of claim 12, wherein the self-timed circuit comprises a memory device communication interface.

14. (Rejected) The system of claim 12, wherein the self-timed circuit comprises a peripheral device communication interface.

15. (Rejected) The system of claim 12, wherein the self-timed circuit comprises a network communication interface.

16. (Rejected) An apparatus comprising:

a substrate;

a self-timed circuit formed on the substrate, the self-timed circuit to operate at a target circuit frequency;

a target timing circuit formed on the substrate, the target timing circuit to generate a signal having a frequency related to the target circuit frequency;

a leakage timing circuit formed on the substrate, the leakage timing circuit having a leakage current and the leakage timing circuit to generate a signal having a frequency related to the leakage current; and

a control unit to receive the signal having the frequency related to the target circuit frequency and the signal having the frequency related to the leakage current and to generate a control signal for application to the substrate, the control signal to maintain a substantially constant ratio between the frequency related to the target circuit frequency and the frequency related to the leakage current.

17. (Rejected) The apparatus of claim 16, wherein the substrate comprises silicon.

18. (Rejected) The apparatus of claim 17, wherein the target circuit comprises an interface circuit.

19. (Rejected) The apparatus of claim 18, wherein the target ring oscillator comprises a ring oscillator coupled to a counter.

20. (Rejected) The apparatus of claim 19, wherein the leakage ring oscillator comprises a delay line.

21. (Allowed) An apparatus comprising:

a substrate;

a synchronous circuit formed on the substrate, the synchronous circuit to operate at a target circuit frequency;

a target timing circuit formed on the substrate, the target timing circuit including voltage control, the target timing circuit to generate a signal having a frequency related to the target circuit frequency;

a leakage timing circuit formed on the substrate, the leakage timing circuit including voltage control, the leakage timing circuit having a leakage current and the leakage timing circuit to generate a signal having a frequency related to the leakage current;

a control unit to receive the signal having a frequency related to the target circuit frequency, the signal having a frequency related to the leakage current, and to generate a control signal for application to the substrate, the control signal to maintain a substantially constant ratio between the frequency related to the target circuit frequency and the frequency related to the leakage current;

a power source to provide a potential to the synchronous, the target timing circuit, and the leakage timing circuit; and

a potential control unit to receive the signal having the frequency related to the target circuit frequency and the signal having the frequency related to the leakage current and to generate a potential control signal to provide to the power source to adjust the potential.

22. (Allowed) The apparatus of claim 21, wherein the substrate comprises silicon.

23. (Allowed) The apparatus of claim 22, wherein the synchronous circuit comprises a processor.

24. (Allowed) The system of claim 23, wherein the processor comprises a very long instruction word processor.

25. (Allowed) The apparatus of claim 21, wherein the control unit includes a low-leakage control signal to set the target circuit to a low leakage state.

26. (Rejected) A method comprising:

generating a first signal related to a target circuit frequency;

generating a second signal related to a leakage current; and

adjusting a control signal applied to a substrate to maintain a substantially constant frequency ratio between the first signal and the second signal.

27. (Rejected) The method of claim 26, further comprising for a processor formed on the substrate and having an operating frequency and a supply voltage, changing the supply voltage to maintain a relationship between the target circuit frequency and the operating frequency.

28. (Rejected) The method of claim 26, further comprising for a communications circuit formed on the substrate, activating a transceiver in the communications circuit.

29. (Rejected) The method of claim 26, further comprising processing the target circuit frequency and a target ring oscillator frequency to generate a potential control signal to adjust a potential applied to a target ring oscillator, a leakage ring oscillator, and a target circuit that operates at the target circuit frequency.

30. (Rejected) The method of claim 29, further comprising for a communications circuit formed on the substrate, activating a transceiver in the communications circuit.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.